REMARKS

Applicants not that the Examiner has failed to provide any explanation of his rejection of claim 5 under 35 USC 102(e). Applicants are therefore unable to respond to the Examiners rejection of claim 5. Applicants respectfully request an explanation of the Examiners rejection of claim 5 or withdrawal of his rejection of claim 5.

The Examiner rejected claims 1, 3 and 7 under 35 U.S.C. 112 (second paragraph).

The Examiner rejected claims 1-3, 5-13, 15-18 and 20 under 35 U.S.C. §102(e) as being unpatentable over Lin et al. (2005/0242430 A1).

The Examiner rejected claim 14 under 35 U.S.C. 103 as being unpatentable over Lin et al. in view of Chen et al. (29004/0187304 A1).

The Examiner rejected claims 4, 19 and 214 under 35 U.S.C. 103 as being unpatentable over Lin et al. in view remarks.

Applicants respectfully traverse the §112, §102(e) and §103 rejections with the following arguments.

35 USC § 112

The Examiner rejected claims 1, 3 and 7 under 35 U.S.C §112, (second) paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regards as the invention, stating:

"In claim 1, the limitation '---first capping layer thin enough---' is vague and indefinite. It is not clear which thin is desired. In claims 3 and 7, the limitation '---first capping layer sufficiently thick---' is vague and indefinite. It is not clear which thick is desired. The remaining claims are dependent from the above rejected claims and therefore also considered indefinite."

In response, Applicants have amended claims 1, 3 and 7 to remove the limitation "thin enough" from claim 1 and "sufficiently thick" from claims 3 and 7.

35 USC § 102

As to claim 1, the Examiner states that "Lin et al. teach a method of manufacturing an interconnect, comprising: (a) providing a substrate 10; (b) forming a dielectric layer 14 on said substrate; (c) forming a wire 18C/18D in said dielectric layer, a top surface of said wire coplanar with a top surface of said dielectric layer (figs IA- lE and related texts); (d) forming a first capping layer 22 on said top surface of said wire and said top surface of said dielectric layer, said first capping layer thin enough (SiN, 50 A-50 OA) in paragraph [0021] to allow penetration of said first capping layer by a point of a conductive probe tip in order to make electrical contact to said wire18C/1 8D; and (e) after step (d) forming a second capping layer 24 on a top surface of said first capping layer."

Applicants contend that claim 1, as amended, is not anticipated by Lin et al. because Lin et al. does not teach each and every feature of claim 1. For example Lin et al. does not teach "pushing a conductive probe tip through said first capping layer in order to make electrical contact to said wire, and then afterwards removing said conductive probe tip from said wire and said first capping layer." Applicant respectfully point the purpose of first capping layer 22 of Lin et al. is to act as "a glue layer" to increase adhesion between the top surface of wire 18C/18D and the second capping layer 24 (see Lin et al Abstract and paragraphs 21-25). Lin et al. teaches only forming first capping layer 22, treating the surface of first capping layer 22 with a plasma or e-beam and then immediately forming second capping layer 24 on top of first capping layer 22. Lin et al. does not teach "pushing a conductive probe tip through said first capping layer in order to make electrical contact to said wire" nor does Lin et al. teach any electrical probing of the wire 18C/18D at all.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Lin et al. and is in condition for allowance. Since claims 2-21 and 61-65 depend from claim 1, Applicants respectfully maintain that claims 2-21 and 61-65 are likewise in condition for allowance.

As to claim 9, the Examiner states that Lin et al teaches "wherein said first capping layer and said second capping layer independently include one or more layer of materials selected from the group consisting of Si.sub.xN.sub.y, Si.sub.xC.sub.y, SiC.sub.xH.sub.y, SiC.sub.xO.sub.yN.sub.z and SiC.sub.xN.sub.y. (Fig. 1E and related texts, [0025])".

Applicants contend that claim 9, as amended, is not anticipated by Lin et al. because Lin et al. does not teach each and every feature of claim 9. For example Lin et al. does not teach "wherein said first capping layer and said second capping layer each include two or more layers, each layer of said two or more layers of said first and second capping layers independently including materials selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN."

Applicants respectfully point first capping layer 22 of Lin et al. taught as a single layer of material and second capping layer 24 of Lin et al. is taught as single layer of material.

Based on the preceding arguments, Applicants respectfully maintain that claim 9 is not unpatentable over Lin et al. and is in condition for allowance.

As to claim 17, the Examiner states that Lin et al. teaches "further including between steps (d) and (e), cryogenically (100-400 C) cleaning said top surface of said first capping layer [0023]."

First, Applicants respectfully point out Lin et al. is not teaching a cryogenic cleaning in paragraph 23 but a plasma teaching. Lin et al paragraph 23 actually states "The glue layer **plasma** process treatment may be carried out at a temperature from about 0 °C to about 400 °C, more preferably about 100 °C to about 400 °C, most preferably from about 325 °C to about 375 °C. Applicants maintain a plasma process is incompatible with a cryogenic process. Further, a person of ordinary skill the art would know that cryogenic cleaning and plasma cleaning are unrelated processes.

Second, the Examiner appears to have concluded a cryogenic process inherently includes temperatures of 0 °C or higher without any support for that conclusion. In refutation Applicants respectfully submit:

(1) The National Institute of Standards and Technology at Boulder, Colorado have chosen to consider the field of cryogenics as that involving temperatures below –180 °C (93.15 K). (Wikipedia - The Free Dictionary, http://en.wikepedia.org/wiki/Cryogenic)

(2) Cryogenics is a branch of physics (or engineering) that studies the production of very low temperatures (below –150 °C, –238 °F or 123 K) and the behavior of materials at those temperatures. (Wikipedia - The Free Dictionary, http://en.wikepedia.org/wiki/Cryogenic)

Based on the preceding arguments, Applicants respectfully maintain that claim 17 is not unpatentable over Lin et al. and is in condition for allowance.

As to claim 18, the Examiner states Lin et al. teaches "further including between steps (c) and (d), cleaning (by CMP [0020]) said top surface of said wire and said top surface of said dielectric layer in a reducing environment."

Applicants point out that CMP is not a cleaning process but a planarizing process and even if construed as such, there is most certainly no teaching of a "reducing environment" as Applicants claim 18 requires.

35 USC § 103 Rejections

As to claims 4, 14, 19 and 21, Applicants have argued *supra* in response to the Examiners § 102(e) rejection of claim 1 that claim 1 is allowable, since claims 4, 14, 19 and 21 depend from claim 1, Applicants respectfully maintain that claims 4, 14, 19 and 21 are not unpatentable over Lin et al. and are in condition for allowance.

As to claim 4, the Examiner states that "Lin et al. teaches the claimed invention as applied to claim 1 except for dielectric layer comprises fluorinated silicon glass and wherein said dielectric layer comprises about 1% o to about 9% by weight of fluorine as cited in current claim. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize dielectric layer comprises fluorinated silicon glass, because it is commonly used to prevent undesirable or detrimental reactions in process of making a conductive interconnection structure."

First, Applicants respectfully point out that the Examiners statement " fluorinated silicon glass is commonly used" is not supported by any evidence and is thus an improper shifting of the burden of proof of prima facie obviousness from the Examiner to Applicants. Second Applicants find the statement "prevent undesirable or detrimental reactions" vague since this statement covers any reaction imaginable and is thus improper.

Based on the preceding arguments, Applicants respectfully maintain that claim 4 is not unpatentable over Lin et al and is in condition for allowance.

As to claim 14, the Examiner states that "Lin et al. teaches the claimed invention as applied to claim 1 except for forming another dielectric layer on a top surface of said second

capping layer, said second capping layer acting as a reactive ion etch stop for etching said another dielectric layer. Chen teaches the step of forming another dielectric layer on a top surface of said second capping layer 360, said second capping layer acting as a reactive ion etch stop for etching said another dielectric layer ([0053] and fig. 3E and related texts). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form another dielectric layer on a top surface of said second capping layer, said second capping layer acting as a reactive ion etch stop for etching said another dielectric layer in Lin 's method in order to form overlaying upper level metal interconnect."

First, Applicants point out that there is no reason to for the second capping layer of Lin et al. to be an etch stop layer since Lin et al. does is not forming any further layers. Lin et al. specifically teaches that the capping layers 24 and 26 do not delaminate from an uppermost inter-metal dielectric (IMD) layer (see Lin et al. paragraph 300).

Second, Applicants maintain the rejection is improper because there is no suggestion in the prior art to combine the references as required by *Karsten Mfg. Corp. v. Cleveland Gulf Co.*, 242 F.3d 1376, 1385, 58 U.S.P,Q.2d 1286, 1293 (Fed. Cir. 2001) which states " In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention." The alleged motivation does originate from prior art but has been supplied by the Examiner. Therefore, the Examiner has not established his prima facie case of obviousness.

Third, formation of damascene wires or sub-etched wires requires breaking through the second capping layer, so making it an etch stop layer adds additional processing steps to Lin et al

that are not required by Lin et al. Further, it is not necessary that the capping layer be an etch stop layer in order to form upper level metal interconnects.

Based on the preceding arguments, Applicants respectfully maintain that claim 14 is not unpatentable over Lin et al. in view of Chen et al. and is in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Gambino et al.

Dated: 08/21/2006

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